

7Z Series 7.0 x 5.0 mm SMD Differential Output Crystal Oscillator

7 : 7.0×5.0×1.45 mm | SMD7050-6P

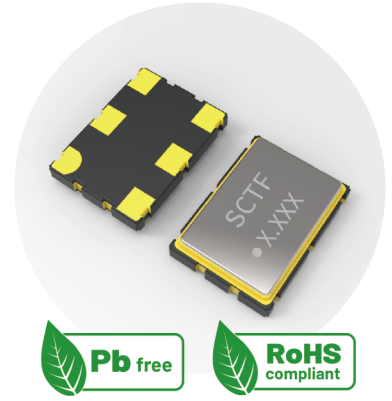
Z : Differential Output Crystal Oscillator(SPXO)

Feature

- Output Types: LVPECL/LVDS/HCSL
- Tri-state function available
- Low Phase Jitter : 0.5pSec max.
- Pb-free/RoHS Compliant

Applications

- Networking and communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH



Frequency Stability & Operating Temperature Range

Temp. \ FT	±20ppm	±25ppm	±30ppm	±50ppm
-20°C to +70°C	△	★	★	★
-40°C to +85°C		△	★	★

★: Available △: Conditional

All condition: Include 25°C tolerance, operating temperature range, input voltage change, aging, load change.

Electrical Specifications

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000, 106.250, 125.000 148.500, 150.000, 155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVPECL				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
Storage Temperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	V _{dd}	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L _{PECL}		50		Ω	V _{dd} - 2.0 V
Current Consumption	I _{cc}			50	mA	90MHz ≤ Freq. < 125MHz
				75		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% V _{dd} to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}	V _{dd} -1.025			V	
Low output voltage	V _{OL}			V _{dd} -1.62	V	
Enable Voltage High (Logic 1)	V _{IH}	0.7V _{dd}			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3V _{dd}	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90			dBc/Hz
	1 KHz		-120			dBc/Hz
	10 KHz		-140			dBc/Hz
Aging	f _{age}			3	ppm	1st. Year at 25°C

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Standard Frequency	Freq.	100.000 ,106.250 ,125.000 148.500 ,150.000 ,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVDS				
Operating Temperature	T_use	-20		+70	°C	
		-40		+85	°C	
Storage Temperature Range	T_stg	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L_LVDS		100		Ω	
Current Consumption	Icc			30	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	Tr / Tf			1	nS	20% Vdd to 80% Level
Start-up Time	T_str			10	mS	To 90% of Final Amplitude
High output voltage	VoH			1.6	V	
Low output voltage	VoL	0.9			V	
Enable Voltage High (Logic 1)	VIH	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	VIL			0.3Vdd	V	
RMS Phase Jitter	TRPJ			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f_age			3	ppm	1st. Year at 25°C

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Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000 ,106.250 ,125.000 148.500 ,150.000 ,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		HCSL				
Operating Temperature	T_use	-20		+70	°C	
		-40		+85	°C	
Storage Temperature Range	T_stg	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L_HCSL		Rs=33 , Rl=50		Ω	
Current Consumption	Icc			35	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	Tr / Tf			1	nS	20% Vdd to 80% Level
Start-up Time	T_str			10	mS	To 90% of Final Amplitude
High output voltage	VoH	0.66			V	
Low output voltage	VoL			0.15	V	
Enable Voltage High (Logic 1)	VIH	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	VIL			0.3Vdd	V	
RMS Phase Jitter	TRPJ			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f_age			3	ppm	1st. Year at 25°C

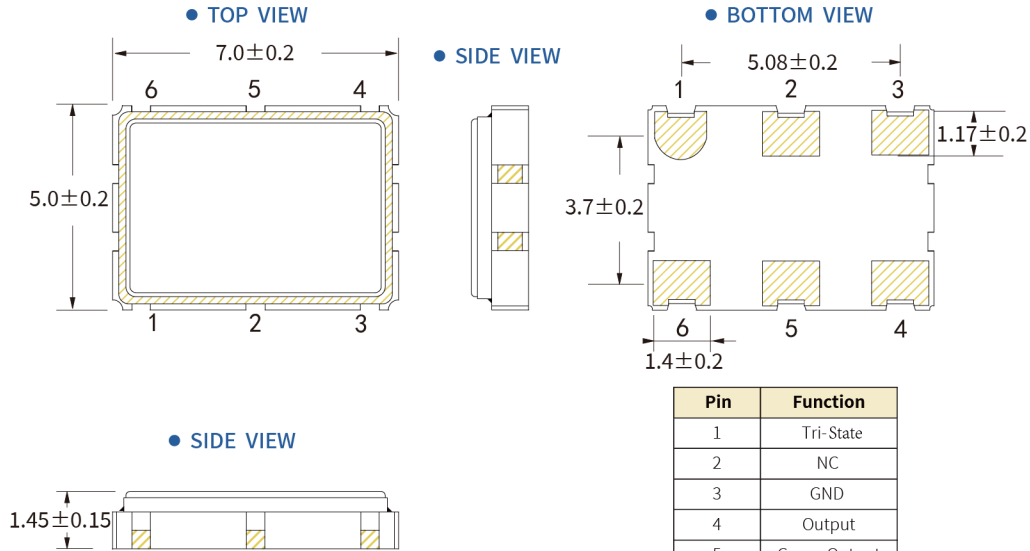
更新日期: 2024年4月10日

7Z Series 7.0 x 5.0 mm SMD Differential Output Crystal Oscillator

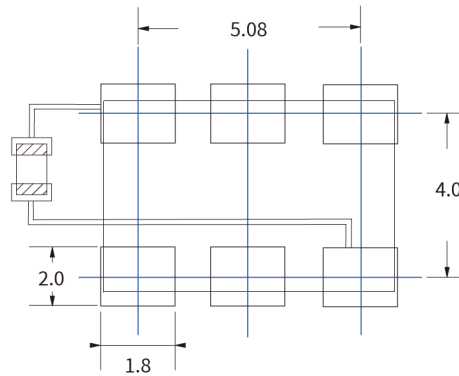
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Z : Differential Output Crystal Oscillator(SPXO)

Dimensions (UNIT:mm)



Solder pad layout (UNIT:mm)



To ensure optimal oscillator performance, place a by-pass capacitor of 0.1μF as close to the part as possible between Vdd and GND pads.

Options and Part Identification : Example SX7DF100.000B20F30DNN

Company	Ceramic Package	Frequency Code [MHZ]	Supply Voltage	Frequency Tolerance	Operating Temperature	Frequency Drift	Output	Current Consumption	Phase Noise
SX	7DF	X.XXX	B	20	F	30	D	N	N
Code Company		Frequency		Code Frequency Tolerance		Code Frequency Drift		Code Current	
SX SCTF		100,000		10 ±10ppm 20 ±20ppm		15 ±15ppm 20 ±20ppm 30 ±30ppm		N Standard	
	Code Ceramic Package		Code Voltage		Code Operating Temperature		Code Output		Code Phase Noise
	7DF 7.0×5.0×1.45mm 5DF 5.0×3.2×1.25mm 3DF 3.2×2.5×0.9mm		D 1.8V H 2.5V B 3.3V		E -20°C ~ +70°C F -40°C ~ +85°C		P LVPECL D LVDS H HCSSL		N Standard

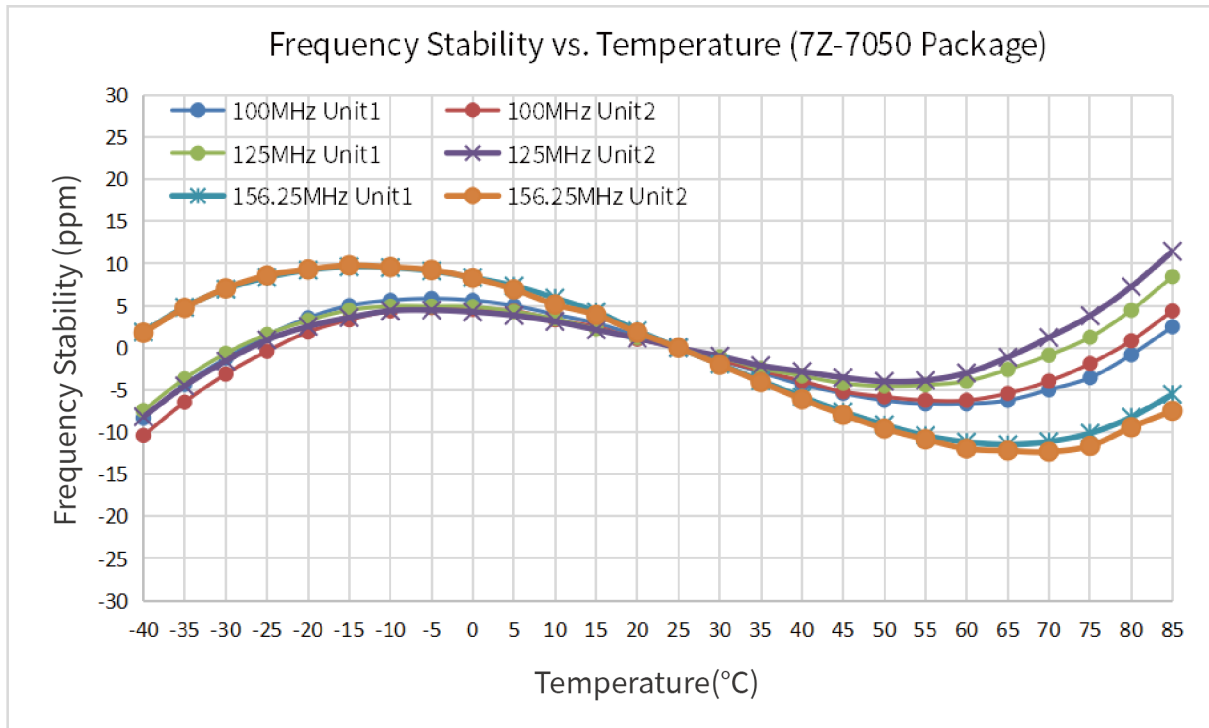
If you have other parameter requirements, you can contact **SCTF** at any time.

7Z Series 7.0 x 5.0 mm SMD Differential Output Crystal Oscillator

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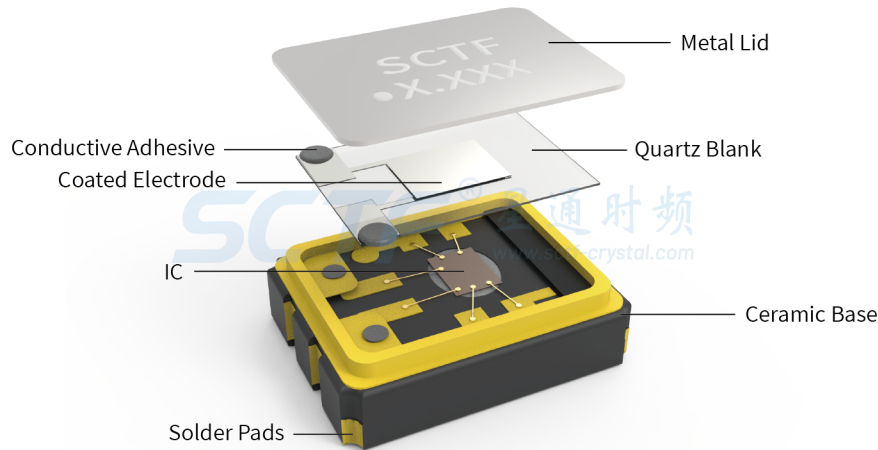
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Frequency Temperature Characteristics

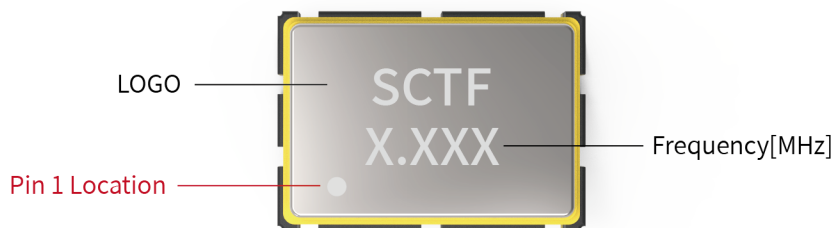


Product Structure & Marking Information

Product Structure



Marking Information

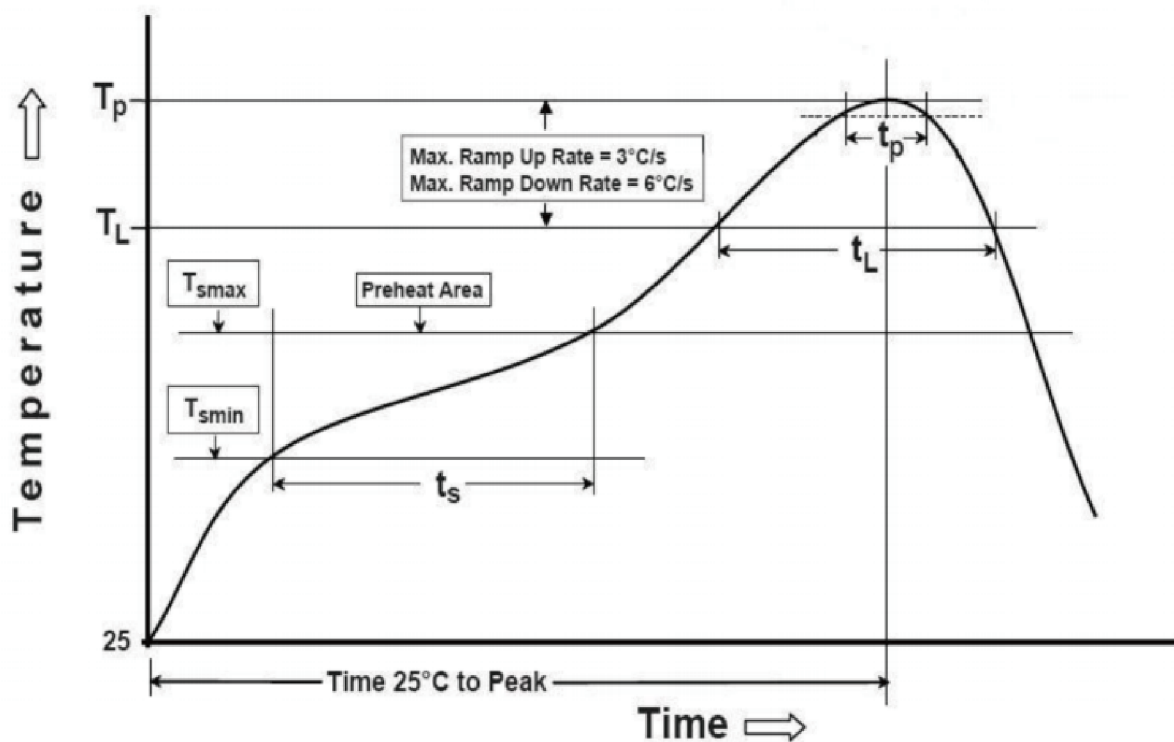


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Suggested Reflow Profile



Profile Feature	Sn - Pb Eutectic Assembly	Preheat / Soak
Preheat / Soak <ul style="list-style-type: none"> ● Temperature Min (Ts min) ● Temperature Max (Ts max) ● Time (Ts min to Ts max) 	100°C 150°C 60-120 seconds	150°C 200°C 60-120 seconds
Ramp - up rate (TL to Tp)	3°C/ second max.	3°C/ second max.
Time maintained above <ul style="list-style-type: none"> ● Liquidous temperature (TL) ● Time (tL) maintained above TL 	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body temperature (Tp)	235°C	260°C
Time within 5° C of the specified classification temperature (Tp)	20 seconds	30 seconds
Ramp - down rate (Tp to TL)	6°C/ second max.	6°C/ second max.
Time 25° C to peak temperature	6 minutes max.	8 minutes max.
Suggest reflow times	2 Times max.	

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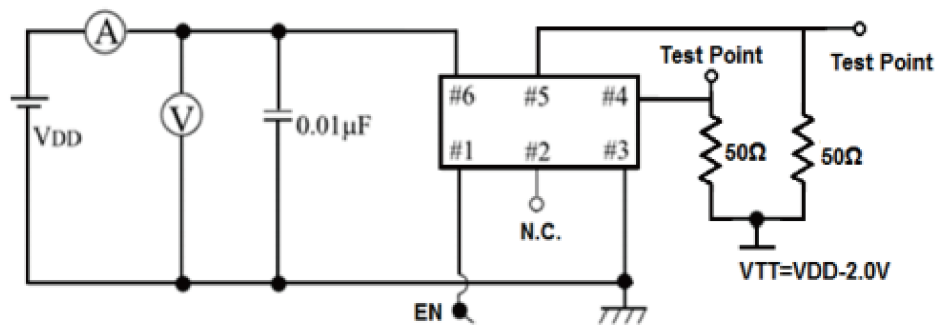
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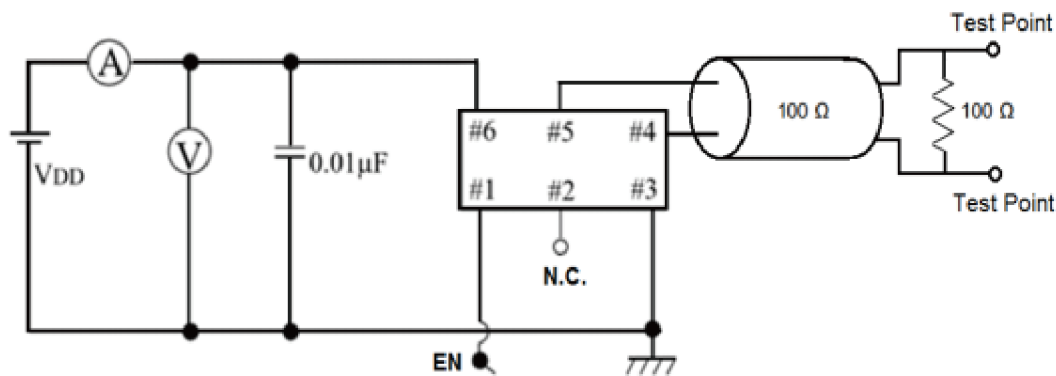
Testing Circuit

- LVPECL



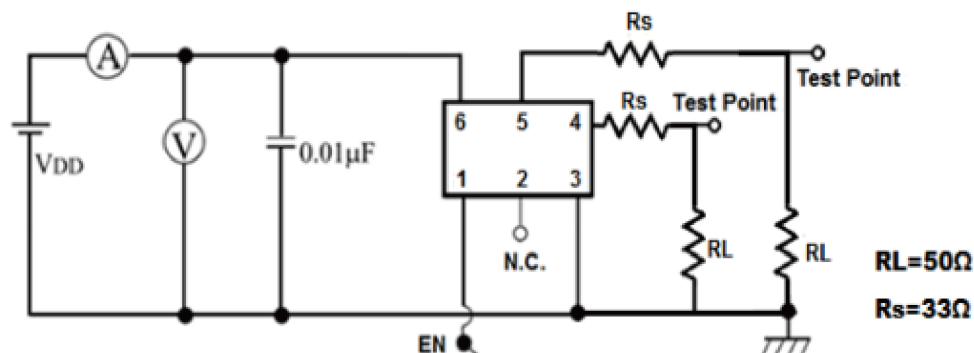
※ Notes: PIN 1 connected to Vdd or floating, the product is working properly;connected to GND,stops working.

- LVDS



※ Notes: PIN 1 connected to Vdd or floating, the product is working properly;connected to GND,stops working.

- HCSL



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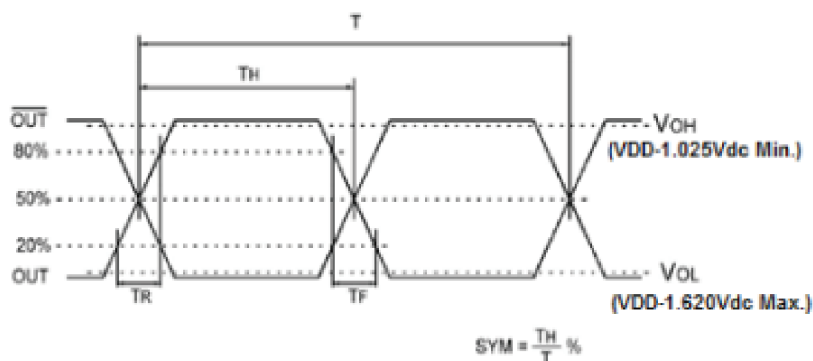
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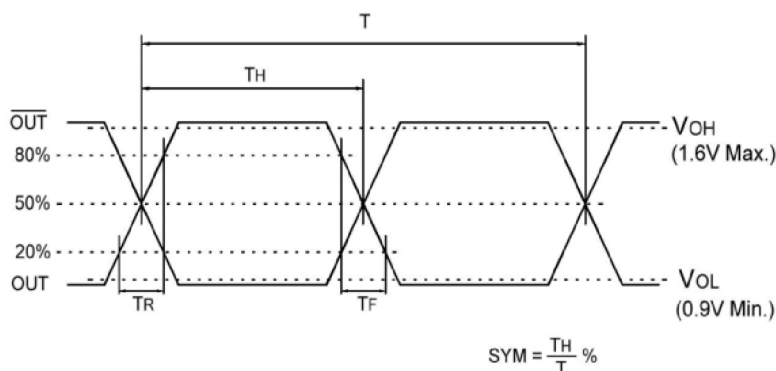
Waveform Conditions

- LVPECL



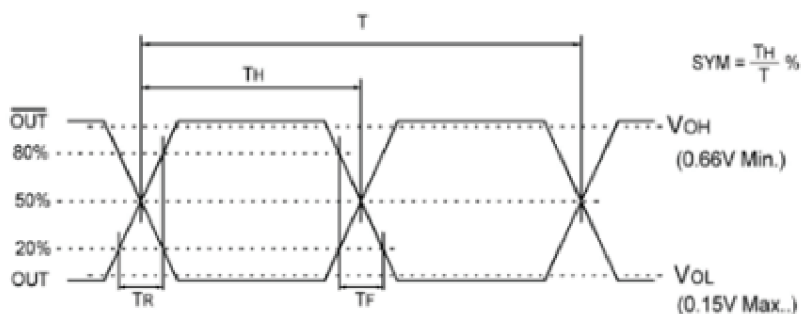
Waveform measurement system should have a min. bandwidth of 5 times the frequency being tested.

- LVDS



Waveform measurement system should have a min. bandwidth of 5 times the frequency being tested.

- HCSL



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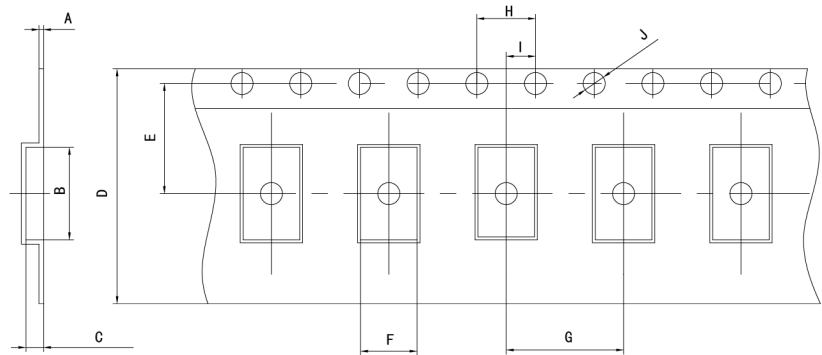
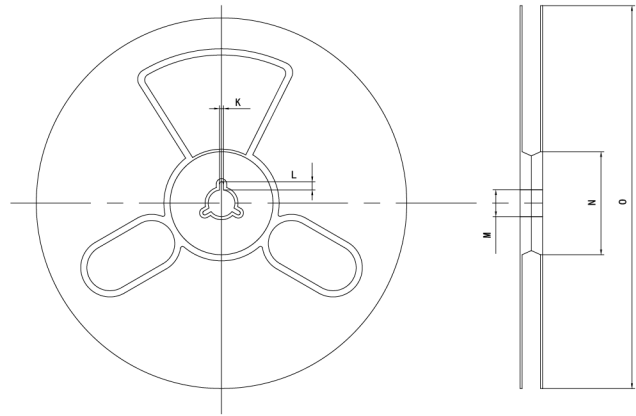
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Packaging Information

T=Tape and reel (1,000pcs/reel)



Pocket Tape Dimensions(mm)

Series	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
7Z	0.3±0.05	7.6±0.1	2.0±0.1	16±0.3	7.5±0.1	5.4±0.1	8.0±0.1	4.0±0.1	2.0±0.1	φ1.5±0.1	2.0±0.2	4.0±1.0	φ13±0.5	φ60±1	φ180±1

Common Frequencies – MHz

7Z Series				
100.000	106.250	125.000	148.500	150.000
155.520	156.250			